IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/212,903, filed August 5, 2002, ~~pending~~ now U.S. Patent 6,611,467, issued August 26, 2003, which is a continuation of application Serial No. 09/977,755, filed October 15, 2001, now U.S. Patent 6,442,086 ~~B1~~, issued August 27, ~~2002,~~ 2002, which is a continuation of application Serial No. 09/897,360, filed July 2, 2001, now U.S. Patent 6,327,201 ~~B2~~, issued December 4, 2001, which is a continuation of application Serial No. 09/583,478, filed May 31, 2000, now U.S. Patent 6,256,242, issued July 3, 2001, which is a continuation of application Serial No. 09/392,154, filed September 8, 1999, now U.S. Patent 6,101,139, issued August 8, 2000, which is continuation of application Serial No. 09/026,244, filed February 19, 1998, now U.S. Patent 6,002,622, issued December 14, 1999.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006]

Once the memory cells attached to the complementary digit lines D0*, D1*, etc. have been tested, the memory cells attached to the true digit lines D0, D1, etc. are tested by firing the row line R1, for example. This causes the memory cells attached to the row line R1 to dump their stored charge from their memory cell capacitors 12 onto the complementary digit lines D0*, D1*, etc. In turn, this causes the sense amplifiers 14 to pull each of the complementary digit lines D0*, D1*, etc. up to the supply voltage V_{CC}, and to pull each of the true digit lines D0, D1, etc. down to ground. As a result, a full V_{CC}-to-ground voltage drop is imposed across NMOS access devices 18 of the memory cells attached to the true digit lines D0, D1, etc. The V_{CC}-~~to~~-to-ground voltage drop is maintained across the NMOS access devices 18 for another predetermined refresh interval of about 150 to 200 ms. This stresses any "leaky" NMOS access devices 18 and causes any such NMOS access devices 18 to lose significant charge from their memory cell capacitors 12 to the true digit lines D0, D1, etc. to which they are attached.

Please replace paragraph number **[0008]** with the following rewritten paragraph:

[0008] This conventional margin testing method thus typically takes two predetermined refresh intervals of about 150 to 200 ms. each to complete. Since row lines in different ~~sub-~~ sub-arrays in a semiconductor memory typically cannot be fired simultaneously because the addressing of the row lines is local to their respective sub-arrays, this conventional method cannot be used on more than one sub-array at a time. As a result, in a semiconductor memory containing four sub-arrays, for example, the conventional method described above takes approximately 1.2 to 1.6 seconds to complete. Because of the large number of semiconductor memories that typically require margin testing during production, it would be desirable to find a margin testing method that can be completed more quickly than the method described above.

Please replace previously numbered paragraph number **[0015]** with the following paragraph **[0014a]**:

[0014a] The inventive margin testing circuitry thus stresses all memory cells in the memory at the same time without the need to fire individual row lines in different sub-arrays. As a result, it substantially reduces the time it takes to complete a margin test of the memory. Also, by positioning the switching circuits within the memory, the inventive margin testing circuitry avoids the cumbersome nature of the external probe pad of prior margin testing devices.

Please replace previously numbered paragraph number **[0016]** with the following paragraph **[0015]**:

[0015] In other embodiments of the invention, a semiconductor memory, an electronic system, and a semiconductor substrate (*e.g.*, a semiconductor wafer) incorporate the inventive margin testing circuitry described above.

Please replace previously numbered paragraph number **[0017]** with the following paragraph **[0016]**:

[0016] In another embodiment of the invention - a method of margin testing a DRAM - a high voltage level is stored in memory cells of the DRAM. Equilibrating circuitry in sense

amplifiers of the DRAM is isolated from an equilibrate bias node of the DRAM and from a cell plate voltage thereon, and a ground voltage from within the DRAM is applied to the equilibrating circuitry in each sense amplifier. Digit line pairs of the DRAM are then equilibrated to the ground voltage using the equilibrating circuitry in each sense amplifier, and the digit line pairs are held at the ground voltage for a predetermined refresh interval in order to stress the memory cells of the DRAM, which are attached to the digit line pairs. After the predetermined refresh interval has passed, all the memory cells of the DRAM are read to identify those that have failed the margin test. The refresh interval may be, for example, about 150 to 200 milliseconds.

Please replace previously numbered paragraph number **[0018]** with the following paragraph **[0017]**:

[0017] In still another embodiment of the invention - a method of testing a semiconductor memory - a substantially identical logic voltage is stored in all memory cells of the semiconductor memory. Also, digit line pairs of the semiconductor memory that are attached to the memory cells are isolated from a digit line equilibrating bias voltage. This is accomplished by deactivating an NMOS transistor coupled between the bias voltage and the digit line pairs, or by failing to activate equilibrate circuitry coupled between the bias voltage and the digit line pairs that normally is activated during memory operations of the semiconductor memory. A stressing voltage from within the semiconductor memory that is substantially different than the logic voltage stored in the memory cells is then applied to all the digit lines of all the digit line pairs at substantially the same time, thereby stressing the memory cells. The digit line pairs are held at the stressing voltage for a predetermined interval, and all the memory cells of the semiconductor memory are then read to identify those that have failed the test.

Please replace previously numbered paragraph number **[0019]** with the following paragraph **[0018]**:

[0018] FIG. 1 is a schematic and block diagram illustrating a conventional method for margin testing a semiconductor memory;

Please replace previously numbered paragraph number **[0020]** with the following paragraph **[0019]**:

[0019] FIG. 2 is a schematic diagram illustrating another prior art method for margin testing a semiconductor memory;

Please replace previously numbered paragraph number **[0021]** with the following paragraph **[0020]**:

[0020] FIG. 3 is a schematic and block diagram illustrating circuitry for margin testing a Dynamic Random Access Memory (DRAM) according to the present invention;

Please replace previously numbered paragraph number **[0022]** with the following paragraph **[0021]**:

[0021] FIG. 4 is a more detailed schematic view of the circuitry of FIG. 3;

Please replace previously numbered paragraph number **[0023]** with the following paragraph **[0022]**:

[0022] FIG. 5 is a block diagram of an electronic system including a memory device that incorporates the DRAM and circuitry of FIG. 3; and

Please replace previously numbered paragraph number **[0024]** with the following paragraph **[0023]**:

[0023] FIG. 6 is a diagram of a semiconductor wafer that incorporates the DRAM and circuitry of FIG. 3.

Please replace previously numbered paragraph number **[0025]** with the following paragraph **[0024]**:

[0024] As shown in FIG. 3, the invention includes margin testing circuitry (see FIG. 4) incorporated into sense amplifiers 30 of a Dynamic Random Access Memory (DRAM) 32 or other semiconductor memory. It should be understood by those having skill in the technical field

of the invention that the margin testing circuitry may be directly connected to digit lines D0, D0*, D1, D1*, etc. of the DRAM 32 instead of being incorporated into the sense amplifiers 30, or may be incorporated into other circuitry of the DRAM 32 that is connected to the digit lines D0, D0*, D1, D1*, etc.

Please replace previously numbered paragraph number **[0026]** with the following paragraph **[0025]**:

[0025] A margin test is performed on the DRAM 32 in accordance with the invention by first storing a supply voltage V_{CC} level in the storage capacitors 34 of the DRAM 32 using the sense amplifiers 30, digit lines D0, D0*, D1, D1*, etc., row lines R0, R1, R2, R3, etc., and NMOS access devices 36 of memory cells of the DRAM 32. An active margin test mode signal GNDDIGTM* then causes the sense amplifiers 30 to ground the digit lines D0, D0*, D1, D1*, etc. for a predetermined refresh interval of about 150 to 200 milliseconds. Of course, longer or shorter refresh intervals may also be used. Grounding the digit lines D0, D0*, D1, D1*, etc. stresses the NMOS access devices 36 with a V_{CC}-to-ground voltage drop, causing any of the NMOS access devices 36 that are leaky to leak charge.

Please replace previously numbered paragraph number **[0027]** with the following paragraph **[0026]**:

[0026] After the predetermined refresh interval has passed, all the memory cells of the DRAM 32 are read. Any that leaked sufficient charge to read out at a low voltage level rather than at the supply voltage V_{CC} level they originally stored are then identified as having failed the margin test.

Please replace previously numbered paragraph number **[0028]** with the following paragraph **[0027]**:

[0027] It should be understood that the invention grounds all digit lines D0, D0*, D1, D1*, etc. at the same time without the need to fire any of the row lines R0, R1, R2, R3, etc. As a

result, the invention margin tests all sub-arrays within the DRAM 32 at the same time, in contrast to the traditional margin test method previously described.

Please replace previously numbered paragraph number **[0029]** with the following paragraph **[0028]**:

[0028] It should also be understood that stressing voltages other than ground may be applied to the digit lines D0, D0*, D1, D1*, etc. during a margin test, and that, accordingly, different voltages may be stored on the storage capacitors 34 to begin the margin test. For example, the storage capacitors 34 may store a ground voltage level while a supply voltage V_{CC} level is uniformly applied to the digit lines D0, D0*, D1, D1*, etc. to stress the NMOS access devices 36.

Please replace previously numbered paragraph number **[0030]** with the following paragraph **[0029]**:

[0029] As shown in FIG. 4, one of the sense amplifiers 30 includes equilibrating NMOS transistors 40 for equilibrating the voltage on the digit lines D0, D0*. During normal memory operations, the margin test mode signal GNDDIGTM* is inactive, which causes an isolating NMOS transistor 42 to be active and couple the equilibrating NMOS transistors 40 to an equilibrate bias node 44 connected to the cell plate voltage DVC2. During the margin test mode, the margin test mode signal GNDDIGTM* is active, causing the isolating NMOS transistor 42 to isolate the equilibrating NMOS transistors 40 from the equilibrate bias node 44, and causing a PMOS switching transistor 46 to turn on and activate an NMOS switching transistor 48, thereby applying a ground voltage to the equilibrating NMOS transistors 40. In response to an active equilibrate signal EQ, the equilibrating NMOS transistors 40 in turn apply the ground voltage to the digit lines D0 and D0* simultaneously.

Please replace previously numbered paragraph number **[0031]** with the following paragraph **[0030]**:

[0030] It should be noted that because the invention does not attempt to isolate the equilibrate bias node 44 from the cell plate voltage DVC2, but rather provides an isolating NMOS transistor 42 for each sense amplifier 30 to individually isolate each pair of digit lines from the equilibrate bias node 44, the invention provides a more reliable margin test method than the known probe pad method previously described, which does attempt to isolate the equilibrate bias node 44 from the cell plate voltage DVC2 and the cell plate.

Please replace previously numbered paragraph number **[0032]** with the following paragraph **[0031]**:

[0031] In an alternative system as described above, in which the switching transistors 46 and 48 are directly connected to digit lines D0 and D0* rather than being connected through equilibrating NMOS transistors 40, or are incorporated into circuitry other than the sense amplifier 30 that is directly connected to the digit lines D0 and D0*, an alternative method for isolating the digit lines D0 and D0* from the equilibrate bias node 44 in accordance with the invention involves not activating the equilibrate signal EQ.

Please replace previously numbered paragraph number **[0033]** with the following paragraph **[0032]**:

[0032] As shown in FIG. 5, an electronic system 50 in accordance with the invention includes an input device 52, an output device 54, a processor device 56, and a memory device 58 incorporating the DRAM 32 of FIG. 3. As shown in FIG. 6, the DRAM 32 of FIG. 3 is fabricated on a semiconductor wafer 60. Of course, it should be understood that semiconductor substrates other than a semiconductor wafer also fall within the scope of the present invention, including, for example, Silicon-on-Sapphire (SOS) substrates, Silicon-on-Glass (SOG) substrates, and Silicon-on-Insulator (SOI) substrates.

Please replace previously numbered paragraph number **[0034]** with the following paragraph **[0033]**:

[0033] Although the present invention has been described with reference to particular embodiments, the invention is not limited to these described embodiments. Rather, the invention is limited only by the appended claims, which include within their scope all equivalent devices or methods that operate according to the principles of the invention as described.